<u>Amendments to the Claims:</u>

This listing of claims will replace all prior versions, and listings, of claims in the application:

<u>Listing of Claims:</u>

1. (Currently amended) A computer system, comprising:

a processor running an operating system; and

a memory subsystem <u>having a redundancy and</u> coupled to said processor, said memory subsystem comprising a memory controller and a plurality of memory modules coupled to said memory controller;

wherein a memory module is present in the computer system but isolated wherein<u>, using the memory subsystem's redundancy,</u> transactions that target said isolated memory module can complete without loss of data and without accessing said isolated memory module, and while isolated, said memory module is tested <u>by one of a system management interrupt (SMI) handler that accesses said isolated memory module via an address in I/O space that is mapped to an address in memory space that corresponds to the isolated memory module or test logic internal to the memory module</u>.

2. (Currently amended) The computer system of claim 1 wherein ~~the memory subsystem comprises redundancy and~~ data is not lost due to the redundancy of the memory subsystem.

3. (Original) The computer system of claim 1 wherein the memory subsystem comprises a RAID subsystem and read and write transactions can be completed that target said isolated memory module without loss of data using data from other memory modules.

4. (Canceled).

5. (Canceled).

6. (Original) The computer system of claim 1 wherein the memory subsystem comprises a mirrored configuration.

7. (Currently amended) The computer system of claim 1 further including ~~an SMI handler that runs code to test a memory module when isolated and said computer system further includes~~ a memory map having a plurality of addresses, a first range of addresses corresponding to said isolated memory module and a second range of addresses that is mapped to said first range to permit said SMI handler access to said isolated memory module to run its code.

8. (Original) The computer system of claim 1 wherein, when isolated, an isolated memory module is isolated upon insertion into said system.

9. (Original) The computer system of claim 1 wherein the plurality of memory modules comprises hot plug modules.

10. (Currently amended) A memory subsystem usable in an electronic system, comprising:

a memory controller; and

a plurality of hot plug memory modules that can be coupled to said memory controller and configured to provide redundancy;

wherein a hot plug memory module may be inserted into said memory subsystem and caused to be inaccessible to an operating system and, based on the redundancy, transactions to said inserted memory module can complete without loss of data and without accessing said isolated memory module, and said inserted memory module, ~~can be tested~~ despite being inaccessible to the operating system, can be tested by one of a system management interrupt (SMI) handler that accesses said inserted memory module via an

address that is mapped to an address corresponding to the isolated memory module or test logic internal to the inserted memory module.

11. (Original) The memory subsystem of claim 10 wherein the memory subsystem's redundancy is from a RAID configuration.

12. (Original) The memory subsystem of claim 11 wherein, when a hot plug memory module is inserted, the inserted memory module tests itself while inaccessible to the operating system.

13. (Original) The memory subsystem of claim 10 wherein the memory subsystem's redundancy is from a mirrored configuration.

14. (Currently amended) A memory subsystem usable in an electronic system, comprising:

a memory controller;

connectors through which a plurality of hot plug memory modules can be coupled to said memory controller;

a means for isolating a newly inserted memory module so as to preclude an operating system from causing data to be written to or read from said newly inserted memory module, yet completing transactions targeting said newly inserted memory module using redundancy of the memory subsystem, and for testing said memory module.

15. (Original) The memory subsystem of claim 14 wherein said means for isolating comprises a RAID memory subsystem.

16. (Original) The memory subsystem of claim 14 wherein said means for isolating comprises a memory map in which a first address range is associated with said newly inserted memory module and the memory map including a

second address range that is mapped to the first address range to permit an interrupt handler to test said memory module.

17. (Currently amended) A method, comprising:

inserting a hot plug memory unit into a memory subsystem having redundancy;

isolating said hot plug memory unit so that transactions targeting said hot plug memory unit can be completed using the redundancy of the memory subsystem, but not completed to the isolated hot plug memory unit; and

testing said hot plug memory unit while said hot plug memory unit is isolated, said testing performed by one of a system management interrupt (SMI) handler that accesses said inserted hot plug memory unit via an address that is mapped to an address corresponding to the inserted hot plug memory or test logic internal to the inserted hot plug memory.

18. (Original) The method of claim 17, wherein upon completing said testing, terminating isolation of said hot plug memory unit to permit access to said hot plug memory unit by read and write transactions under the control of an operating system.

19. (Original) The method of claim 17 wherein testing includes accessing a range of logical address that are re-mapped to a different range of logical addresses that are associated with said isolated hot plug memory unit.